REMARKS

Attached hereto is a fee for one (1) additional claim in excess of the twenty-four claims for which a fee has previously been paid.

Claims 1-16 and 18-25 are pending in the application. This Amendment currently amends claims 1, 5, 7, 10, 16, and 19, and adds new claim 25. Claim 17 is withdrawn from present consideration. No new matter is added to currently amended claims 1, 5, 7, 10, 16, and 19. Claims 1, 5, 7, 10, 16, and 19 are currently amended to merely clarify the subject matter of the claims and in no way narrow the scope of the claims in order to overcome the prior art or for any other statutory purpose of patentability.

Notwithstanding any claim amendments of the present Amendment or those amendments that may be made later during prosecution, Applicants' intent is to encompass equivalents of all claim elements. Reconsideration in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-4 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,939,788 to McTeer. Claims 21 and 22 stand rejected under 35 U.S.C. §103(a) as unpatentable over McTeer in view of U.S. Patent No. 6,225,207 to Parikh. Claims 5-15, 23, and 24 and claims 16 and 18-20 stand rejected under 35 U.S.C. §102(b) as anticipated by Parikh.

The prior art rejections of September 2, 2003 Final Action are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention, as defined in independent claim 1, is directed to a method of forming an interconnect on a semiconductor substrate that comprises forming a relatively narrow first structure through a dielectric formed on a semiconductor substrate, forming a relatively wider second structure through the dielectric, forming a liner in the relatively narrow first structure and the relatively wider second structure, such that a lower portion of the relatively narrow first structure is completely filled by the liner, and forming a metallization over the liner

to completely fill the relatively wider second structure.

The claimed invention, as defined in independent claim 5, is directed to a method of forming an interconnect on a semiconductor substrate that comprises forming a contact through a dielectric formed on a semiconductor substrate, forming troughs into the dielectric, thereby to form a dual damascene structure, depositing a conducting material on the dielectric that completely fills a lower portion of the contact, depositing a metal over the conducting material to completely fill the troughs, removing a portion of the metal, and selectively removing the conducting material.

The claimed invention, as defined in independent claim 16, is directed to a method of forming an interconnect on a semiconductor substrate that comprises forming troughs between first and second metal levels, including a slot, in a dielectric formed on a semiconductor substrate, forming contacts in the dielectric, thereby to form a dual damascene structure, depositing a conducting material on the dielectric, the conducting material completely filling a lower portion of the dual damascene structure, depositing a metal over the conducting material to completely fill the slot and the troughs, removing a portion of the metal, and selectively removing the conducting material.

The conventional method typically attempts to fill substantially both narrow and wide contact structures with copper, thereby requiring additional and costly processing. For example, it is difficult to adequately line contacts for copper filling at contact dimensions below 280 nm and to line contacts reliably below contact opening sizes of less than 320 nm. The conventional methods present a major challenge to dynamic random access memory back-end-of-line (DRAM BEOL) processing when applying copper to line contacts.

Thus, an exemplary embodiment of the present invention may fill substantially narrow structures with a CVD conductive material and wider structures with copper metallization.

II. THE PRIOR ART REJECTIONS

A. The McTeer Reference

The Examiner cites Fig. 16 and column 23 of McTeer for allegedly disclosing a method

of forming an interconnect on a semiconductor substrate (10), comprising: forming relatively narrow first structure at the bottom of the dual damascene structure in a dielectric (14) formed on a semiconductor substrate; forming a relatively wider second structure at the top of the dual damascene structure in the dielectric formed on the semiconductor substrate; forming a liner (2) comprising aluminum and titanium nitride (line 48) in the first and the second structures such that the first structure is substantially filled and the second structure is substantially unfilled; and forming a metallization (3) comprising copper (line 50) over the liner to fill completely the second structure.

Claim 1 recites at least the features of "forming a liner in said relatively narrow first structure and said relatively wider second structure, such that a lower portion of said relatively narrow first structure is completely filled by said liner; and forming a metallization over said liner to completely fill said relatively wider second structure."

Fig. 16 of McTeer clearly shows copper (3) substantially filling both a relatively narrow structure at the bottom of a dual damascene structure in the dielectric (14) and a relatively wider structure at the top of the dual damascene structure in the dielectric. The liner (2) of McTeer does not completely fill the relatively narrow structure at the bottom of a dual damascene structure in the dielectric (14). Hence, McTeer cannot fill substantially narrow structures with a CVD conductive material and wider structures with copper metallization as in an exemplary embodiment of the present invention.

Therefore, McTeer does not disclose, teach or suggest at least the features of "forming a liner in said relatively narrow first structure and said relatively wider second structure, such that a lower portion of said relatively narrow first structure is completely filled by said liner; and forming a metallization over said liner to completely fill said relatively wider second structure," as recited in claim 1.

For at least the reasons outlined above, Applicants respectfully submit that McTeer does not disclose, teach or suggest every feature of independent claim 1. Accordingly, McTeer does not anticipate, or render obvious, the subject matter of independent claim 1 and claims 2-4, which depend from claim 1, under 35 U.S. §102(b). Withdrawal of the rejection of claims 1-4

under 35 U.S. §102(b) as anticipated by McTeer is respectfully solicited.

B. The Parikh Reference

In regard to the rejection of dependent claims 21 and 22, the Examiner alleges that McTeer anticipates independent claim 1, from which depend claims 21 and 22, but lacks forming the relatively narrow first structure not being connected to the relatively wider second structure and forming the wider second structure on the substrate apart from the relatively narrow first structure. The Examiner then cites Parikh for teaching (in col. 11, lines 31 *et seq.* and Fig. 5D (554 and 552)) forming the relatively narrow first structure (554) not being connected to the relatively wider second structure (552) and forming the wider second structure on the substrate apart from the relatively narrow first structure.

Fig. 5D of Parikh results from a via hole 540, power line trench 525, and signal line trenches 536 and 538 being simultaneously filled with a conductive material, such as a metal (col. 11, 25-27). This structure includes a novel triple damascene structure comprising a power line 552 and a signal line 554 having a via plug 556 (col. 11, lines 29-31).

Claim 1 recites at least the features of "forming a liner in said relatively narrow first structure and said relatively wider second structure, such that a lower portion of said relatively narrow first structure is completely filled by said liner; and forming a metallization over said liner to completely fill said relatively wider second structure."

Both the power line 552 and the signal line 554 of Parikh are filled with a single conductive metal, as clearly shown in Fig. 5D. Hence, Parikh does not distinguish between a liner and a metallization and cannot fill substantially narrow structures with a CVD conductive material and wider structures with copper metallization as in an exemplary embodiment of the present invention.

In contrast, both the relatively narrow first structure and the relatively wider second structure contain a liner, while the relatively wider second structure also includes a metallization, which completely fills the relatively wider second structure.

Parikh does not cure the deficiencies of McTeer. As argued above, nowhere does McTeer

disclose, teach or suggest at least the features of "forming a liner in said relatively narrow first structure and said relatively wider second structure, such that a lower portion of said relatively narrow first structure is completely filled by said liner; and forming a metallization over said liner to completely fill said relatively wider second structure," as recited in claim 1. As argued immediately above, nowhere does Parikh disclose, teach or suggest "forming a liner in said relatively narrow first structure and said relatively wider second structure, such that a lower portion of said relatively narrow first structure is completely filled by said liner; and forming a metallization over said liner to completely fill said relatively wider second structure."

For at least the reasons outlined above, Applicants respectfully submit that McTeer and Parikh, either individually or in combination, do not disclose, teach or suggest every feature of independent claim 1. Accordingly, McTeer and Parikh, either individually or in combination, fail to render obvious the subject matter of independent claim 1 and claims 21 and 22, which depend from claim 1, under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 21 and 22 under 35 U.S.C. §103(a) as unpatentable over McTeer in view of Parikh is respectfully solicited.

Claim 5 recites at least the features of "forming troughs into the dielectric, thereby to form a dual damascene structure; depositing a conducting material on the dielectric that completely fills a lower portion of the contact; [and] depositing a metal over the conducting material to completely fill the troughs."

Claim 16 recites at least the features of "forming troughs ... including a slot ... ; forming contacts in the dielectric, thereby to form a dual damascene structure; depositing a conducting material on the dielectric, said conducting material completely filling a lower portion of said dual damascene structure; [and] depositing a metal over the conducting material to completely fill the slot and the troughs."

As argued above, both the power line 552 and the signal line 554 of Parikh are filled with a single conductive metal, as clearly shown in Fig. 5D. Hence, Parikh does not distinguish between a liner and a metallization and cannot fill substantially narrow structures with a CVD conductive material and wider structures with copper metallization as in an exemplary embodiment of the present invention.

In contrast, both the lower portion of the contact and the lower portion of the dual damascene structure of claims 5 and 16, respectively, contain a liner, while the troughs include both a liner and a metallization, which completely fills the troughs.

Therefore, Parikh does not disclose, teach or suggest at least the features of ""forming troughs into the dielectric, thereby to form a dual damascene structure; depositing a conducting material on the dielectric that completely fills a lower portion of the contact; [and] depositing a metal over the conducting material to completely fill the troughs," and "forming troughs ... including a slot ... ; forming contacts in the dielectric, thereby to form a dual damascene structure; depositing a conducting material on the dielectric, said conducting material completely filling a lower portion of said dual damascene structure; [and] depositing a metal over the conducting material to completely fill the slot and the troughs," as recited in independent claims 5 and 16 respectively.

For at least the reasons outlined above, Applicants respectfully submit that Parikh does not disclose, teach or suggest every feature of independent claims 5 and 16. Accordingly, Parikh does not anticipate, or render obvious, the subject matter of independent claims 5 and 16, and claims 6-15, 23, 24, and claims 17-20, which depend from claims 5 and 16, respectively, under 35 U.S. §102(b). Withdrawal of the rejections of claims 5-15, 23, and 24 and of claims 16-20 under 35 U.S. §102(b) as anticipated by Parikh is respectfully solicited.

III. CONCLUSION

In view of the foregoing, Applicant submits that claims 1-16 and 18-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to withdraw the rejections and pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner may contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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